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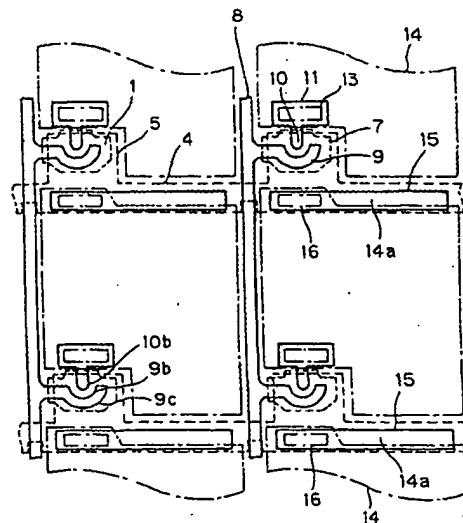
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(54) **TRANSISTOR AND DISPLAY COMPRISING IT**

(57) A transistor has a source electrode and a drain electrode formed with a predetermined interval secured in between on a semiconductor layer formed to perspective overlap a gate electrode. The source and drain electrodes are each longer in their lengthwise direction than in their widthwise direction. The source electrode has a recessed portion formed therein to allow the tip portion of the drain electrode in. The semiconductor layer protrudes out of the gate electrode to form a portion that does not overlap the gate electrode but overlaps the source electrode and a portion that does not overlap the gate electrode but overlaps the drain electrode. Thus, the protruding portion that overlaps the source electrode and the protruding portion that overlaps the drain electrode are separated from each other by the gate electrode so as to be independent of each other. This prevents short-circuiting between the source and drain that results when the portions of the semiconductor islands protruding out of the gate electrode become conductive through a photoelectric effect brought about by the light that travels past the gate electrode or by another cause.

FIG.8



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## Description

### Technical field

[0001] The present invention relates to a transistor, and to a display provided with such a transistor. More specifically, the present invention relates to transistors formed on a substrate so as to form an array, and to a display device having pixel electrodes formed so as to correspond individually to such transistors so that display is controlled pixel by pixel by way of those pixel electrodes.

### Background art

[0002] Commercially available display devices are classified into tube-type display devices, such as CRTs, and flat display devices, such as liquid crystal display devices, EL display devices, and plasma display devices. A flat display device is composed essentially of an aggregation of pixels, and display on it is controlled pixel by pixel so as to produce an overall image. In a flat display device, for example a liquid crystal display device, an array of thin-film transistors are formed on a glass substrate so that display pixels are driven individually by those transistors.

[0003] Fig. 11 shows the structure of a thin-film transistor (hereinafter referred to as a "TFT") that is conventionally used in a liquid crystal display device. In the TFT shown in the figure, on top of a gate electrode G, a semiconductor layer SI of, for example, silicon is formed with an insulating film interposed in between, and then, further on top, a source electrode S and a drain electrode D, both rectangular in shape as seen in a plan view, are arranged side by side with a predetermined interval secured in between. Ideally, the source and drain electrodes S and D should be formed in the designed positions. Occasionally, however, they are formed in deviated positions as shown in Figs. 12 and 13. If, as shown in Fig. 12, the source and drain electrodes S and D deviate in the vertical direction of the figure while maintaining equal overlaps with the gate electrode G, the areas (hatched in the figure) over which the source and drain electrodes S and D overlap the gate electrode G remain unchanged, and thus the parasitic capacitance of the TFT remains almost unchanged. However, if, as shown in Fig. 13, the deviation occurs in the horizontal direction of the figure, one of the source and drain electrodes S and D comes to overlap the gate electrode G over a larger area than the other. This results in a great variation in the parasitic capacitance.

[0004] Based on what has been described thus far, one can recognize the need to reduce variations in the parasitic capacitance of thin-film transistors, in particular those used to drive display pixels, and the need to achieve uniform image quality on a display device of which the display pixels are driven by transistors.

## Disclosure of the invention

[0005] According to the present invention, in a transistor having a source electrode and a drain electrode formed side by side with a predetermined interval secured in between on a semiconductor layer formed so as to perspectively overlap a gate electrode, the source and drain electrodes are each longer in their lengthwise direction than in their widthwise direction, the source electrode has a recessed portion formed therein to allow the tip portion of the drain electrode in, the semiconductor layer protrudes out of the gate electrode to form a portion that does not overlap the gate electrode but overlaps the source electrode and a portion that does not overlap the gate electrode but overlaps the drain electrode, and the protruding portion that overlaps the source electrode and the protruding portion that overlaps the drain electrode are separated from each other by the gate electrode so as to be independent of each other. In this structure, the drain electrode is longer in its lengthwise direction than in its widthwise direction, i. e., elongate, and its tip is allowed in the recess formed in the source electrode. This makes it possible to reduce the area over which the drain electrode, the semiconductor layer, and the gate electrode perspectively overlap one another. Thus, it is possible to reduce parasitic capacitance and thereby reduce leak current. Moreover, it is possible to prevent short-circuiting between the source and drain that results when the portions of the semiconductor layer protruding out of the gate electrode become conductive through an photoelectric effect brought about by the light that travels past the gate electrode or by another cause.

[0006] Alternatively, according to the present invention, in a transistor having a source electrode and a drain electrode formed side by side with a predetermined interval secured in between on a semiconductor layer formed so as to perspectively overlap a gate electrode, the edge of the drain electrode that faces the source electrode is rounded, the semiconductor layer protruding out of the gate electrode to form a portion that does not overlap the gate electrode but overlaps the source electrode and a portion that does not overlap the gate electrode but overlaps the drain electrode, and the protruding portion that overlaps the source electrode and the protruding portion that overlaps the drain electrode are separated from each other by the gate electrode so as to be independent of each other. In this structure, it is possible to reduce the difference between the actual shape of the drain electrode from its designed shape, and thereby overcome the problems of variations in the area of the drain electrode and thus variations in parasitic capacitance, and also variations in the interval between the source and drain electrodes, all resulting from the corners being rounded unexpectedly. The drain electrode, of which the rounded edge faces the source electrode, makes it possible to reduce the area over which it perspectively overlaps the semiconductor layer

and the gate electrode. Thus, it is possible to reduce parasitic capacitance and thereby reduce leak current. Moreover, it is possible to prevent short-circuiting between the source and drain that results when the portions of the semiconductor layer protruding out of the gate electrode become conductive through an photoelectric effect brought about by the light that travels past the gate electrode or by another cause.

[0007] Alternatively, according to the present invention, in a transistor having a source electrode and a drain electrode formed side by side with a predetermined interval secured in between on a semiconductor layer formed so as to perspectively overlap a gate electrode, the edge of the drain electrode that faces the source electrode describes a convex curve, the edge of the source electrode that faces the drain electrode describing a concave curve, the semiconductor layer protruding out of the gate electrode to form a portion that does not overlap the gate electrode but overlaps the source electrode and a portion that does not overlap the gate electrode but overlaps the drain electrode, and the protruding portion that overlaps the source electrode and the protruding portion that overlaps the drain electrode are separated from each other by the gate electrode so as to be independent of each other. In this structure, the tip portion of the drain electrode is surrounded by the curved channel. This makes it possible to secure a comparatively long total channel length. The drain electrode, of which the convex-curved edge faces the concave-curved edge of the source electrode, makes it possible to reduce the area over which it perspectively overlaps the semiconductor layer and the gate electrode. Thus, it is possible to reduce parasitic capacitance and thereby reduce leak current. Moreover, it is possible to prevent short-circuiting between the source and drain that results when the portions of the semiconductor layer protruding out of the gate electrode become conductive through an photoelectric effect brought about by the light that travels past the gate electrode or by another cause.

[0008] Alternatively, according to the present invention, in a transistor having a source electrode and a drain electrode formed side by side with a predetermined interval secured in between on a semiconductor layer formed so as to perspectively overlap a gate electrode, the edge of the drain electrode that faces the source electrode describes a convex arc, the edge of the source electrode that faces the drain electrode and the opposite edge of the source electrode describe concave and convex arcs, respectively, that are concentric with the arc described by the edge of the drain electrode, the semiconductor layer protruding out of the gate electrode to form a portion that does not overlap the gate electrode but overlaps the source electrode and a portion that does not overlap the gate electrode but overlaps the drain electrode, and the protruding portion that overlaps the source electrode and the protruding portion that overlaps the drain electrode are separated from each other by the gate electrode so as to be independent of

each other. In this structure, it is possible to make the channel width uniform and thereby enhance the characteristics of the transistor. Forming opposite edges of the source electrode so that they describe concentric concave and convex arcs helps make its width uniform and narrow, and thus helps reduce the influence of parasitic capacitance. The drain electrode, of which the convex-arc-shaped edge faces the concave-arc-shaped edge of the source electrode, makes it possible to reduce the area over which it perspectively overlaps the semiconductor layer and the gate electrode. Thus, it is possible to reduce parasitic capacitance and thereby reduce leak current. Moreover, it is possible to prevent short-circuiting between the source and drain that results when the portions of the semiconductor layer protruding out of the gate electrode become conductive through an photoelectric effect brought about by the light that travels past the gate electrode or by another cause.

[0009] According to the present invention, in any of the transistors described above, the semiconductor layer may have a profile that runs along profiles of the source and drain electrodes.

[0010] In this structure, the semiconductor layer is less likely to receive light. This helps reduce variations in the various characteristics of the transistors.

[0011] According to the present invention, in a display device that achieves display by using any of the transistors described above, gate conductors and source conductors are arranged in a grid-like configuration, the transistors are located at the intersections between the gate and source conductors, and the drain electrodes of the transistors are arranged substantially parallel to the source conductors. In this structure, even if the positions of the source and drain electrodes deviate in the direction parallel to the source conductors, the gate-drain parasitic capacitance varies only slightly.

[0012] According to the present invention, in a display device that achieves display by using any of the transistors described above, source conductors and gate conductors are arranged in a grid-like configuration, the transistors are located at the intersections between the source and gate conductors, and the drain electrodes of the transistors are arranged substantially perpendicularly to the source conductors. In this structure, even if the positions of the source and drain electrodes deviate in the direction perpendicular to the source conductors, the gate-drain parasitic capacitance varies only slightly. Moreover, when the source and drain electrodes are formed, accurate positioning is required only in the direction perpendicular to the source conductors, and not so accurate positioning is required in the direction parallel to the source conductors.

[0013] According to the present invention, in a display device that achieves display by using any of the transistors described above, the transistors, together with pixel electrodes connected thereto, are arranged in the cells sectioned off by the gate and source conductors, auxiliary capacitance electrodes sandwiched between a gate

insulating film and a protective film from above and from below are arranged between the gate conductor of each stage and the pixel electrode of the next stage arranged so as to overlap the gate conductor, contact holes are formed in the protective film lopsidedly in the side of each stage where the transistors are formed so as to permit the auxiliary capacitance electrodes to connect to the pixel electrodes, and cuts are formed at the edges of the pixel electrodes located above the auxiliary capacitance electrodes in the side of each stage opposite to where the contact holes are formed. These cuts help widen the interval between the pixel electrode of one stage and that of the next, and thus helps prevent short-circuiting between adjacent pixel electrodes and the resulting degradation in display quality.

### Brief description of drawings

#### [0014]

Fig. 1 is a plan view showing an outline of the structure of the TFT array of a first embodiment of the invention.

Fig. 2 is a sectional view taken along line A-A shown in Fig. 1.

Fig. 3 is a plan view schematically showing the structure of the TFT of the first embodiment.

Fig. 4 is a plan view showing the array structure of the TFTs of the first embodiment.

Fig. 5 is a plan view showing an outline of the structure of the TFT array of a second embodiment of the invention.

Fig. 6 is a sectional view taken along line B-B shown in Fig. 1.

Fig. 7 is a plan view schematically showing the structure of the TFT of the second embodiment.

Fig. 8 is a plan view showing the array structure of the TFTs of the second embodiment.

Fig. 9 is a plan view schematically showing the structure of the TFT of a third embodiment of the invention.

Fig. 10 is a plan view showing the array structure of the TFTs of the third embodiment.

Fig. 11 is a plan view schematically showing the structure of a conventional TFT.

Fig. 12 is a plan view similar to Fig. 11, showing another state.

Fig. 13 is a plan view similar to Fig. 11, showing still another state.

### Best mode for carrying out the invention

[0015] Hereinafter, embodiments of the present invention will be described with reference to the drawings.

[0016] In a first embodiment of the invention, a plurality of TFTs 1 having an inverted staggered structure are arranged in a matrix-like configuration so as to form a TFT array 2. These are structured as described below

with reference to Figs. 1 and 2.

[0017] The TFT array 2 has a plurality of gate conductors 4, extending in the horizontal direction of Fig. 1, formed at predetermined intervals on a substrate 3 of, for example, no-alkali glass. From the gate conductors 4, gate electrodes 5 branch off at predetermined intervals. The gate electrodes 5 are covered with a gate insulating film 6 of, for example, silicon nitride (SiNx). On top of the gate insulating film 6, a semiconductor layer is formed in an insular pattern, i.e., as semiconductor islands 7, so as to perspectively (i.e., as seen in a plan view) overlap the gate electrodes 5. The semiconductor islands 7 are formed of an amorphous silicon layer.

[0018] After the formation of the semiconductor islands 7, a plurality of source conductors 8 are formed at predetermined intervals perpendicularly to the gate conductors 4. For each of the cells sectioned off by the gate and source conductors 4 and 8 arranged in a grid-like formation, more precisely, for each of the intersections between the gate and source conductors 4 and 8, one TFT 1 is arranged. From the source conductors 8, source electrodes 9 branch off at the same pitch at which the gate conductors 4 are arranged. Beside each of the source electrodes 9, a drain electrode 10 is formed with a predetermined interval secured in between. The drain electrode 10, at its base, connects to a contact electrode 11 that makes contact with a pixel electrode.

[0019] The TFT array 2, including the semiconductor islands 7, source electrodes 9, drain electrodes 10, and other parts, is covered with a protective film 12 of, for example, silicon nitride (SiNx). In this protective film 12, contact holes 13 are formed that lead to contact electrodes 11. Moreover, contiguous with each TFT 1, a transparent pixel electrode 14 made of ITO, IZO, or the like is formed. The pixel electrodes 14 are arranged in a matrix-like formation so as to correspond, one-to-one, to the TFTs 1, and connect to the corresponding TFTs 1 through the contact holes 13. In a display device of a reflective type, the pixel electrodes 14 may be formed of a reflective film of, for example, a metal.

[0020] Next, with reference to Figs. 3 and 4, the structure of the TFT 1 of the first embodiment will be described.

[0021] As shown in Fig. 3, both the source electrode 9 and the drain electrode 10 are elongate, i.e., longer in their lengthwise direction than in their widthwise direction. The lengthwise direction of the source electrode 9 is perpendicular to the source conductor 8, and the lengthwise direction of the drain electrode 10 is parallel to the source conductor 8. The drain electrode 10 has its tip portion 10a arranged so as to face one edge of the source electrode 9 with a predetermined interval secured in between.

[0022] The greater parts of both the source and drain electrodes 9 and 10 perspectively overlap the semiconductor island 7, and perspectively overlap the gate electrode 5 with the semiconductor island 7 and the gate

insulating film 6 interposed in between. Both the source and drain electrodes 9 and 10 are so arranged that their lengthwise direction perpendicularly crosses an edge of the gate electrode 5. Parts of the source and drain electrodes 9 and 10 are located outside the semiconductor island 7. The part of the source electrode 9 located outside the semiconductor island 7 connects to the source conductor 8, and the part of the drain electrode 10 located outside the semiconductor island 7 connects to the contact electrode 11.

**[0023]** The source electrode 9 has a recessed portion 9a formed in its edge facing the drain electrode 10 to allow the tip portion 10a of the drain electrode 10 in. Between the tip portion 10a of the drain electrode 10 and the recessed portion 9a of the source electrode 9, a channel having a predetermined gap (i.e., the channel width) is formed. Quite naturally, this channel is not linear in shape, but has a nonlinear shape that runs along the profile of the recessed portion 9a.

**[0024]** The parasitic capacitance of the TFT 1 results principally from the portions of the source and drain electrodes 9 and 10 in which they perspective overlap the gate electrode 5 with the gate insulating film 6 and the semiconductor island 7 interposed in between. In particular, the parasitic capacitance resulting from the overlap between the drain electrode 10 and the gate electrode 5 greatly influences the pixel voltage, causing variations in it. In the structure shown in Fig. 3, this gate-drain parasitic capacitance is reduced, and variations in it also are reduced for the reasons described below.

**[0025]** The parasitic capacitance itself is reduced in the following way. As described above, the drain electrode 10 is elongate, i.e., longer in its lengthwise direction than in its widthwise direction, and its tip portion is allowed in the recessed portion 9a formed in the source electrode 9. This helps reduce the area over which the drain electrode 10 overlap the semiconductor island 7 and the gate electrode 5, and thus helps reduce the parasitic capacitance. This also helps reduce leak current. Moreover, the source and drain electrodes 9 and 10 (these are formed of the same metal simultaneously) are arranged side by side in the vertical direction of the figure, and therefore, even if their positions deviate slightly in the horizontal direction of the figure, the gate-drain parasitic capacitance remains unchanged. By contrast, if the positions of the source and drain electrodes 9 and 10 deviate in the vertical direction of the figure, the area over which the drain electrode 10 overlaps the gate electrode 5 varies slightly. Here, the fact that the lengthwise direction of the drain electrode 10 perpendicularly crosses an edge of the gate electrode 5 proves to be advantageous. Specifically, that edge of the gate electrode 5 crosses the drain electrode 10 in the direction of the shorter sides thereof, and therefore, even if the place at which the edge crosses the drain electrode 10 deviates in the lengthwise direction thereof, the area over which the drain electrode 10 overlaps the gate electrode 5 varies only slightly. The advantage

of this structure will be clear when compared with a structure in which the drain electrode 10 is arranged perpendicularly to its arrangement in the embodiment being discussed, i.e., an edge of the gate electrode 5 crosses the drain electrode 10 in the lengthwise direction thereof and the place at which the edge crosses the drain electrode 10 deviates in the direction of the shorter sides thereof. In this way, even if the drain electrode 10 deviates in its lengthwise direction, the area over which the drain electrode 10 overlaps the gate electrode 5 varies only slightly, resulting in reduced variations in the gate-drain parasitic capacitance.

**[0026]** This advantage, i.e., reduced variations in the area over which the drain electrode 10 overlaps the gate electrode 5 even in case of deviation of the source and the drain electrodes 9 and 10 in the vertical direction of the figure, results from the fact that the drain electrode 10 has an elongate shape along the vertical direction of the figure. This shape of the drain electrode 10, however, also has the disadvantage of shortening the total length of the channel between the source and drain electrodes 9 and 10. To overcome this, in the TFT 1 of the first embodiment, the source electrode 9 has the recessed portion 9a formed in it in order to form a channel that has a nonlinear shape surrounding the tip portion 10a. This makes it possible to secure a comparatively long total channel length.

**[0027]** All over the area over which the source and drain electrodes 9 and 10 overlap the gate electrode 5, the semiconductor island 7 is interposed in between. Where the source electrode 9 crosses an edge of the gate electrode 5, the semiconductor island 7 protrudes slightly out of the gate electrode 5, forming a protruding portion in which the semiconductor island 7 does not overlap the gate electrode 5 but overlaps the source electrode 9. Likewise, where the drain electrode 10 crosses an edge of the gate electrode 5, the semiconductor island 7 protrudes slightly out of the gate electrode 5, forming a protruding portion in which the semiconductor island 7 does not overlap the gate electrode 5 but overlaps the drain electrode 10. This helps reduce variations in the parasitic capacitance formed between the source and drain electrodes 9 and 10 and the gate electrode 5. The protruding portion on the source electrode 9 side and that on the drain electrode 10 side are separated from each other by the gate electrode 5 so as to form insular patches that are independent of each other. This prevents short-circuiting between the source and drain that results when the portions of the semiconductor island 7 protruding out of the gate electrode 5 become conductive through a photoelectric effect brought about by the light that travels past the gate electrode 5 or by another cause.

**[0028]** Fig. 4 shows how a plurality of TFTs 1, each structured as described above, are combined individually with pixel electrodes 14 to form an array. A liquid crystal display device can be built by arranging such a TFT array 2, with reduced variations in the parasitic ca-

capacitance of the TFTs 1 constituting it, as one of the two substrates arranged so as to face each other with liquid crystal sealed in between. This makes it possible to achieve display with less unevenness resulting from variations in parasitic capacitance. Even in a case where the TFT 1 is provided additionally with auxiliary capacitance to alleviate the influence of variations in parasitic capacitance, the required auxiliary capacitance can be minimized. This helps minimize the area over which the auxiliary capacitance element shields light and thereby maximize the aperture ratio of the liquid crystal display device.

[0029] Despite the merits mentioned above, the TFT 1 of the first embodiment still leaves room for improvement. Specifically, the shape of the tip portion 10a of the drain electrode 10 has the following disadvantage. When exposed, the tip portion 10a, having sharp corners, tends to be baked on with round corners. In particular, its portions smaller than exposure resolution are likely to be deformed from the designed shapes, and how they are deformed is indefinite. This makes variations likely in the drain-gate parasitic capacitance. Moreover, variations are likely also in the interval between the source and drain electrodes 9 and 10, i.e., in the channel width. These problems are overcome in the TFT 1 of a second embodiment of the invention shown in Figs. 5 to 8.

[0030] Many of the elements constituting the TFT 1 of the second embodiment are common to the first embodiment. Therefore, in the second embodiment, such elements as are common to the first embodiment are identified with the same reference numerals and symbols, and their explanations will not be repeated. The same applies to the third embodiment, which will be described later.

[0031] In the TFT 1 of the second embodiment, the edge of the drain electrode 10 facing the source electrode 9, i.e., the edge of its tip portion 10b, has rounded corners. To give it rounded corners, the edge of the tip portion 10b is so formed as to describe a convex curve. In the figure, as the most typical example of a convex curve, a convex arc is adopted. The corners here are rounded by exposing a predetermined pattern. The corners are rounded with a radius greater than the resolution of exposure equipment. This helps reduce the difference of the actual shape of the drain electrode 10 from its designed shape, and thereby overcome the problems of variations in the area of the drain electrode 10 and thus variations in parasitic capacitance, and also variations in the interval between the source and drain electrodes 9 and 10, all resulting from the corners being rounded unexpectedly.

[0032] Accordingly, a recessed portion 9b having a concave curve is formed in the edge of the source electrode 9 facing the drain electrode 10. In the figure, as the most typical example of a concave curve, a concave arc is adopted. Thus, the channel formed between the tip portion 10b of the drain electrode 10 and the re-

cessed portion 9b of the source electrode 9 is curved, specifically arc-shaped.

[0033] The edge 9c of the source electrode 9 opposite to the recessed portion 9b has a convex curve. In the figure, as the most typical example of a convex curve, a convex arc is adopted. Here, the convex arc of the tip portion 10b of the drain electrode 10, the concave arc of the recessed portion 9b of the source electrode 9, and the convex arc of the edge 9c thereof are concentric. Thus, the arc-shaped channel formed between the drain and source electrodes 10 and 9 has a uniform width. The source electrode 9, too, has a uniform width between the recessed portion 9b and the edge 9c. Making the source-drain interval, i.e., channel width, uniform in this way helps obtain satisfactory characteristics in the TFT 1.

[0034] In the TFT 1, by minimizing the area over which the drain electrode 10 overlaps the gate electrode 5 and the semiconductor island 7, it is possible to reduce the influence of parasitic capacitance. Likewise, by minimizing the area over which the source electrode 9 overlaps the gate electrode and the semiconductor island 7, it is possible to reduce the influence of parasitic capacitance. Forming a recessed portion 9b having a concave curve (arc) in the source electrode 9, giving the opposite edge 9c thereof a convex curve (arc), and making the width of the source electrode 9 between the recessed portion 9b and the edge 9c uniform and as small as possible as described above helps reduce the influence of parasitic capacitance.

[0035] In the description above, the use of the terms "arc" and "concentric" is not intended to mean geometrically exact circles. Any curves similar to circles, for example ellipses, serve the purpose, as long as they permit rounding of corners with a radius greater than the resolution of exposure equipment.

[0036] For maximum effect, the above-described advance rounding of corners with a radius greater than exposure resolution is preferably applied where deformation has the greatest influence on parasitic capacitance and on channel condition, specifically between the drain and source electrodes 10 and 9, in particular between the tip portion 10b of the drain electrode 10 and the recessed portion 9b of the source electrode 9. Though with less effect, it is advisable to apply the rounding of corners elsewhere. For example, it may be applied, to name a few, to the pixel electrode 14 itself, to the contact electrode 11 itself, to where the contact electrode 11 and the drain electrode 10 are connected together, to where the source electrode 9 and the source conductor 8 are connected together, to the gate electrode 5 itself, and to where the gate electrode 5 and the gate conductor 4 are connected together.

[0037] In the TFT 1 of the second embodiment also, where the source electrode 9 crosses an edge of the gate electrode 5, the semiconductor island 7 protrudes slightly out of the gate electrode 5, forming a protruding portion in which the semiconductor island 7 does not

overlap the gate electrode 5 but overlaps the source electrode 9. Likewise, where the drain electrode 10 crosses an edge of the gate electrode 5, the semiconductor island 7 protrudes slightly out of the gate electrode 5, forming a protruding portion in which the semiconductor island 7 does not overlap the gate electrode 5 but overlaps the drain electrode 10. This helps reduce variations in the parasitic capacitance formed between the source and drain electrodes 9 and 10 and the gate electrode 5. The protruding portion on the source electrode 9 side and that on the drain electrode 10 side are separated from each other by the gate electrode 5 so as to form insular patches that are independent of each other. This prevents short-circuiting between the source and drain that results when the portions of the semiconductor island 7 protruding out of the gate electrode 5 become conductive through an photoelectric effect brought about by the light that travels past the gate electrode 5 or by another cause.

[0038] Fig. 8 shows how a plurality of TFTs 1, each structured as described above, are combined individually with pixel electrodes 14 to form an array. The TFT array 2 of the second embodiment differs from that of the first embodiment in some respects. The differences will be described below.

[0039] In the TFT 1 of the second embodiment, on top of the gate insulating film 6, an auxiliary capacitance electrode 15 is formed. The auxiliary capacitance electrode 15 is formed, after the formation of the semiconductor island 7, simultaneously with the source conductor 8, source electrode 9, drain electrode 10, and contact electrode 11. The auxiliary capacitance electrode 15, too, is covered, from above, with the protective film 12. In the protective film 12, a contact hole 16 is formed that leads to the auxiliary capacitance electrode 15. Thus, the pixel electrode 14, at one end, connects to the TFT 1 through the contact hole 13 and, at the other end, connects to the auxiliary capacitance electrode 15 through the contact hole 16.

[0040] The gate insulating film 6 and the protective film 12, formed below the pixel electrode 14, are removed except where they connect to the pixel electrode 14 and to the electrodes and conductors formed below it. Thus, the greater part of the pixel electrode 14 makes direct contact with the substrate 3. By removing the insulating and protective films formed below the pixel electrode 14 in this way, it is possible to increase the amount of transmitted light.

[0041] The pixel electrode 14 is arranged so as not to perspectively overlap the gate electrode 5, which shields light. The pixel electrode 14 has a cut formed at one corner thereof to allow the TFT 1 in. This leaves a space in which to place the TFT 1 between the pixel electrode 14 of one stage and the pixel electrode 14 of the next stage. Instead of arranging the TFT 1 and the pixel electrode 14 in such a way that they do not overlap each other in this way, it is also possible, in a case where an interlayer insulation layer is formed to cover the TFT

1, to arrange the TFT 1 and pixel electrode 14 in such a way that they perspectively overlap each other.

[0042] The auxiliary capacitance electrode 15 is sandwiched between the gate insulating film 6 and the protective film 12, from above and from below, and is arranged so as to perspectively overlap the gate conductor 4 without protruding out of the gate conductor 4. The length of the auxiliary capacitance electrode 15 is roughly equal to or slightly smaller than the dimension of the pixel electrode 14 in the direction of the shorter sides thereof (i.e., in the direction in which the gate conductor 4 extends).

[0043] It is advisable that the contact hole 16 be formed in such a way as to be located within half the dimension of the pixel electrode 14 in the direction of the shorter sides thereof, preferably within the dimension of the TFT 1 as projected on the gate conductor 4, or alternatively within the dimension of the source electrode 9 as projected on the gate conductor 4, or alternatively within the dimension of the contact electrode 11 as projected on the gate conductor 4. The contact hole 16 so sized is formed lopsidedly in that side of the pixel electrode 14 where the TFT 1 is formed. Thus, while the pixel electrode 14 needs to reach the contact hole 16 in that side of the pixel electrode 14 where the contact hole 16 is formed, there is no such requirement in that side of the pixel electrode 14 in which the contact hole 16 is not formed, and therefore, in this side of the pixel electrode 14, the shape of the pixel electrode 14 can be designed comparatively freely. By exploiting this freedom in design, a cut 14a through which the auxiliary capacitance electrode 15 is exposed is formed in that side of the pixel electrode 14 where the contact hole 16 is formed. This cut 14a helps widen the interval between the pixel electrode of one stage and that of the next, and thus helps prevent short-circuiting between adjacent pixel electrodes and the resulting degradation in display quality.

[0044] Figs. 9 and 10 show the structure of the TFT 1 of a third embodiment of the invention. In this TFT 1 also, both the source electrode 9 and the drain electrode 10 are elongate, i.e., longer in their lengthwise direction than in their widthwise direction. This embodiment is characterized in that the source and drain electrodes 9 and 10 are arranged in such a way that their lengthwise directions are aligned on a straight line. Thus, both the source and drain electrodes 9 and 10 have their lengthwise direction running perpendicularly to the source conductor 8 and parallel to the gate conductor 4.

[0045] Here also, the greater parts of both the source and drain electrodes 9 and 10 perspectively overlap the semiconductor island 7, and perspectively overlap the gate electrode 5 with the semiconductor island 7 and the gate insulating film 6 interposed in between. Both the source and drain electrodes 9 and 10 are so arranged that their lengthwise direction perpendicularly crosses an edge of the gate electrode 5. The source electrode 9, in its portion protruding out of the semicon-

ductor island 7, connects to the source conductor 8, and the drain electrode 10, in its portion protruding out of the semiconductor island 7, connects to the contact electrode 11.

[0046] The tip portion 10c of the drain electrode 10 faces the tip portion of the source electrode 9 with a predetermined interval (channel width) secured in between. Here, as in the second embodiment, the edge of the tip portion 10c of the drain electrode 10 is so formed as to describe a convex arc as the most typical example of a convex curve. The source electrode 9 has a recessed portion 9d formed in its tip portion to allow the tip portion 10c of the drain electrode 10 in, and the recessed portion 9d is so formed as to describe a concave arc as the most typical example of a concave curve. Thus, the channel formed between the tip portion 10c of the drain electrode 10 and the recessed portion 9d of the source electrode 9 is arc-shaped. The edge 9e of the source electrode 9 opposite to the recessed portion 9d is so formed as to describe a convex arc. The convex arc of the tip portion 10c of the drain electrode 10, the concave arc of the recessed portion 9d of the source electrode 9, and the convex of the edge 9e thereof are concentric.

[0047] In this structure, the source and drain electrodes 9 and 10 are aligned on a straight line in their lengthwise direction, and are so shaped as to be symmetric about their mid line extending in their lengthwise direction. This makes it easy to form the electrodes exactly as designed. This is particularly true with the source electrode 9.

[0048] Moreover, the source and drain electrodes 9 and 10 are not only aligned on a straight line in their lengthwise direction, but are also arranged perpendicularly to the source conductor 8 so that their lengthwise direction perpendicularly crosses an edge of the gate electrode 5. Accordingly, even if the positions of those electrodes deviate slightly in the vertical direction of the figure (i.e., parallel to the source conductor 8), the gate-drain parasitic capacitance remains unchanged. By contrast, if the positions of the source and drain electrodes 9 and 10 deviate in the horizontal direction of the figure (perpendicularly to the source conductor 8), the areas over which the source and drain electrodes 9 and 10 overlap the gate electrode 5 vary. That is, the gate-drain parasitic capacitance varies. Thus, while accurate positioning is required in the horizontal direction of the figure, not so accurate positioning is required in the vertical direction of the figure.

[0049] On the other hand, if the source conductor 8 and the pixel electrode 14 are too close to each other, even when the protective film 12 is interposed between them, the voltage applied to the source conductor 8 jumps to the pixel electrode 14, and causes defective display. Therefore, when the source conductor 8 and the pixel electrode 14 are formed, high accuracy is required in positioning in the horizontal direction of the figure so that they are arranged with the designed interval. In the third embodiment, the source and drain electrodes 9

and 10 of the TFT 1 are arranged in the horizontal direction of the figure, and thus, when the source conductor 8 and the pixel electrode 14 are formed, high accuracy is required only in the horizontal direction of the figure. That is, high accuracy is required in only one direction, and this makes fabrication easier than in a case where accuracy is required in two directions, i.e., in the vertical and horizontal directions.

[0050] In the TFT 1 of the third embodiment, as in the TFT 1 of the second embodiment, the recessed portion 9d of the source electrode 9 has a concave curve (arc) and the edge 9e opposite thereto has a convex curve (arc). This helps make the width of the source electrode 9 between the recessed portion 9d and the edge 9e uniform and as small as possible, and thus helps alleviate the influence of parasitic capacitance.

[0051] The semiconductor island 7 has to be located only in a region in which it overlaps the source and drain electrodes 9 and 10 and the channel region, and it is rather undesirable to locate the semiconductor island 7 elsewhere. This is to minimize the leak current produced through a photoelectric effect when light is incident on the semiconductor island 7. The portion of the semiconductor island 7 that overlaps the gate electrode 5 does not receive the light from a backlight because the gate electrode 5 shields the light. Even this portion may receive the light reflected from a color filter array arranged so as to face the TFT array 2. Therefore, it is advisable to remove as much of the unnecessary portion of the semiconductor island 7 as possible even in the region in which it overlaps the gate electrode 5. Accordingly, the semiconductor island 7 is so shaped that its profile runs along the profiles of the source and drain electrodes 9 and 10, with the portion of the semiconductor island 7 away from the source and drain electrode 9 and 10 cut off. This makes the semiconductor island 7 less likely to receive light, and thus helps reduce variations in the various characteristics of the TFT 1. This design technique of giving the semiconductor island 7 a profile that runs along the profiles of the source and drain electrodes 9 and 10 is applied to the TFTs 1 of the first and second embodiments also.

[0052] In the TFT 1 of the third embodiment also, the channel between the source and drain electrodes 9 and 10 has a nonlinear shape, and this makes it possible to secure a comparatively long total channel length. Where the source electrode 9 crosses an edge of the gate electrode 5, the semiconductor island 7 protrudes slightly out of the gate electrode 5, forming a protruding portion in which the semiconductor island 7 does not overlap the gate electrode 5 but overlaps the source electrode 9. Likewise, where the drain electrode 10 crosses an edge of the gate electrode 5, the semiconductor island 7 protrudes slightly out of the gate electrode 5, forming a protruding portion in which the semiconductor island 7 does not overlap the gate electrode 5 but overlaps the drain electrode 10. This helps reduce variations in the parasitic capacitance formed between the source and

drain electrodes 9 and 10 and the gate electrode 5. The protruding portion on the source electrode 9 side and that on the drain electrode 10 side are separated from each other by the gate electrode 5 so as to form insular patches that are independent of each other. This prevents short-circuiting between the source and drain that results when the portions of the semiconductor island 7 protruding out of the gate electrode 5 become conductive through an photoelectric effect brought about by the light that travels past the gate electrode 5 or by another cause.

[0053] The TFT arrays 2 of the embodiments described above can be used on one of the two substrates that constitute a display device that uses transistors to drive display pixels, such as a liquid crystal display device having liquid crystal sealed between two substrates or an organic or inorganic EL display device. The embodiments described above all deal with TFTs having an inverted staggered structure using amorphous silicon; however, the TFT array may be formed by using TFTs of any other type, such as TFTs having a noninverted staggered structure or TFTs having semiconductor islands formed of polycrystalline silicon.

#### Industrial applicability

[0054] The present invention finds wide application in display devices that use transistors to drive display pixels, and is useful in realizing display devices that achieves stable, high-quality display.

#### Claims

1. A transistor having a source electrode and a drain electrode formed side by side with a predetermined interval secured in between on a semiconductor layer formed so as to perspectively overlap a gate electrode, **characterized by**
  - the source and drain electrodes being each longer in a lengthwise direction thereof than in a widthwise direction thereof,
  - the source electrode having a recessed portion formed therein to allow a tip portion of the drain electrode in,
  - the semiconductor layer protruding out of the gate electrode to form a portion that does not overlap the gate electrode but overlaps the source electrode and a portion that does not overlap the gate electrode but overlaps the drain electrode,
  - the protruding portion that overlaps the source electrode and the protruding portion that overlaps the drain electrode are separated from each other by the gate electrode so as to be independent of each other.
2. A transistor having a source electrode and a drain electrode formed side by side with a predetermined interval secured in between on a semiconductor layer formed so as to perspectively overlap a gate electrode, **characterized by**
  - an edge of the drain electrode that faces the source electrode being rounded,
  - the semiconductor layer protruding out of the gate electrode to form a portion that does not overlap the gate electrode but overlaps the source electrode and a portion that does not overlap the gate electrode but overlaps the drain electrode,
  - the protruding portion that overlaps the source electrode and the protruding portion that overlaps the drain electrode are separated from each other by the gate electrode so as to be independent of each other.
3. A transistor having a source electrode and a drain electrode formed side by side with a predetermined interval secured in between on a semiconductor layer formed so as to perspectively overlap a gate electrode, **characterized by**
  - an edge of the drain electrode that faces the source electrode describing a convex curve,
  - an edge of the source electrode that faces the drain electrode describing a concave curve,
  - the semiconductor layer protruding out of the gate electrode to form a portion that does not overlap the gate electrode but overlaps the source electrode and a portion that does not overlap the gate electrode but overlaps the drain electrode,
  - the protruding portion that overlaps the source electrode and the protruding portion that overlaps the drain electrode are separated from each other by the gate electrode so as to be independent of each other.
4. A transistor having a source electrode and a drain electrode formed side by side with a predetermined interval secured in between on a semiconductor layer formed so as to perspectively overlap a gate electrode, **characterized by**
  - an edge of the drain electrode that faces the source electrode describing a convex arc,
  - an edge of the source electrode that faces the drain electrode and an opposite edge of the source electrode describing concave and convex arcs, respectively, that are concentric with the arc described by the edge of the drain electrode,
  - the semiconductor layer protruding out of the gate electrode to form a portion that does not overlap the gate electrode but overlaps the source electrode and a portion that does not overlap the gate electrode but overlaps the drain electrode,
  - the protruding portion that overlaps the source electrode and the protruding portion that overlaps the drain electrode are separated from each other by the gate electrode so as to be independent of each other.

5. A transistor as claimed in one of claims 1 to 4, further **characterized by**  
the semiconductor layer having a profile that runs along profiles of the source and drain electrodes. 5
6. A display device that achieves display by using transistors as claimed in one of claims 1 to 5, **characterized by**  
gate conductors and source conductors being arranged in a grid-like configuration, 10  
the transistors being located at intersections between the gate and source conductors,  
the drain electrodes of the transistors being arranged substantially parallel to the source conductors. 15
7. A display device that achieves display by using transistors as claimed in one of claims 1 to 5, **characterized by** 20  
source conductors and gate conductors being arranged in a grid-like configuration,  
the transistors being located at intersections between the source and gate conductors,  
the drain electrodes of the transistors being arranged substantially perpendicularly to the source conductors. 25
8. A display device as claimed in claim 6 or 7, further **characterized by** 30  
the transistors, together with pixel electrodes connected thereto, being arranged in cells sectioned off by the gate and source conductors,  
auxiliary capacitance electrodes sandwiched between a gate insulating film and a protective film from above and from below being arranged between the gate conductor of each stage and the pixel electrode of a next stage arranged so as to overlap the gate conductor, 35  
contact holes being formed in the protective film lopsidedly in a side of each stage where the transistors are formed so as to permit the auxiliary capacitance electrodes to connect to the pixel electrodes, 40  
cuts being formed at edges of the pixel electrodes located above the auxiliary capacitance electrodes in a side of each stage opposite to where the contact holes are formed. 45

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FIG.1

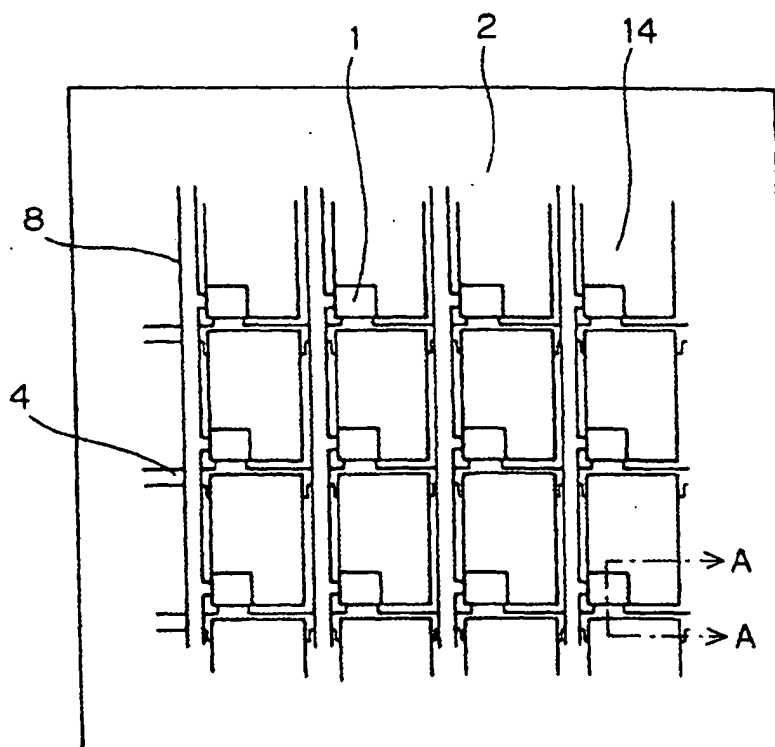


FIG.2

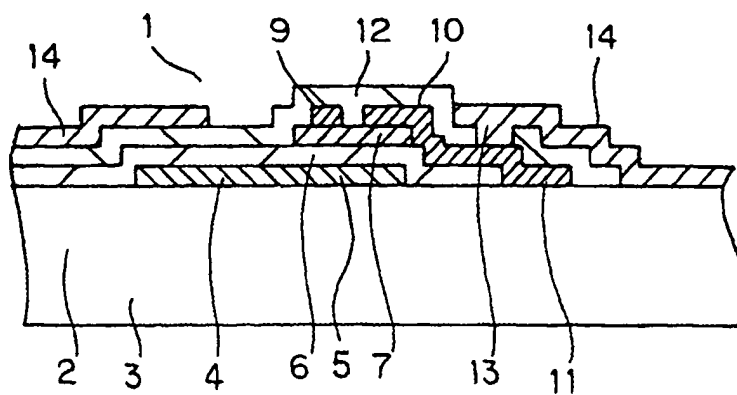


FIG.3

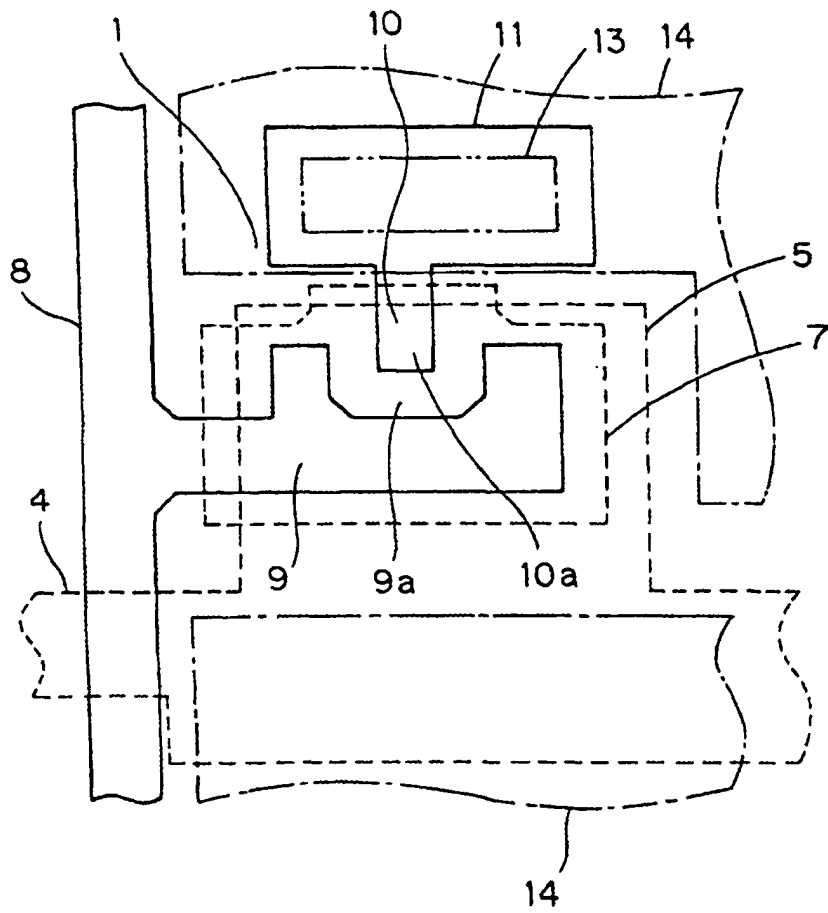


FIG.4

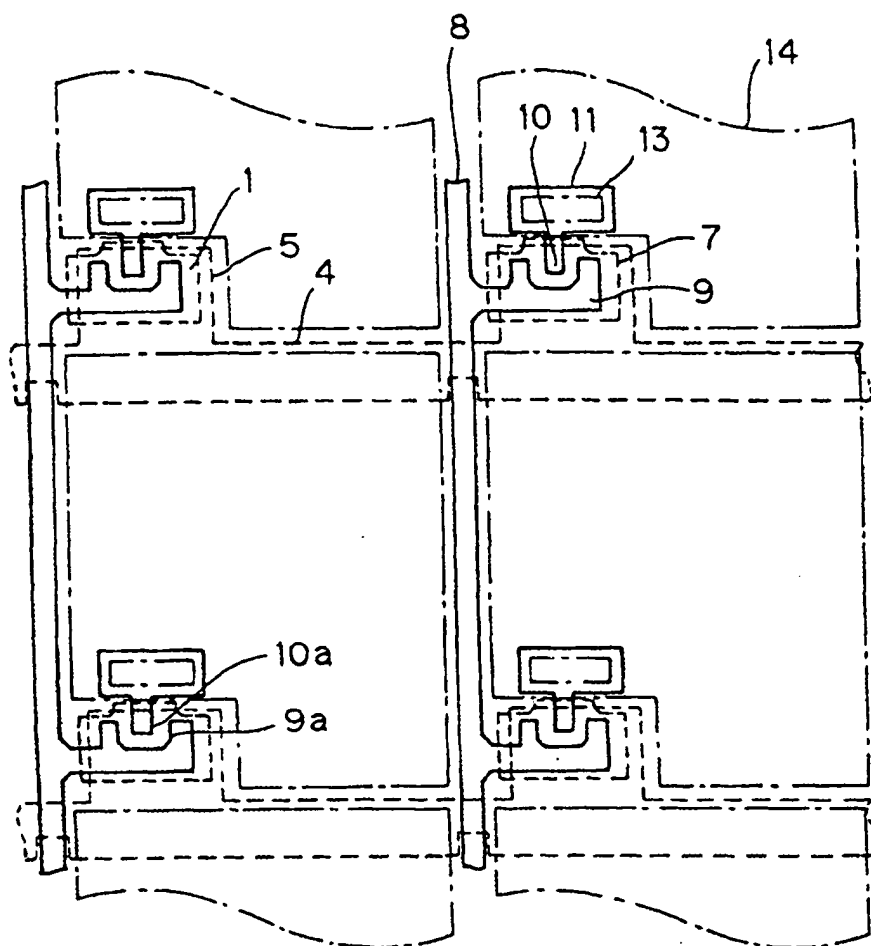


FIG.5

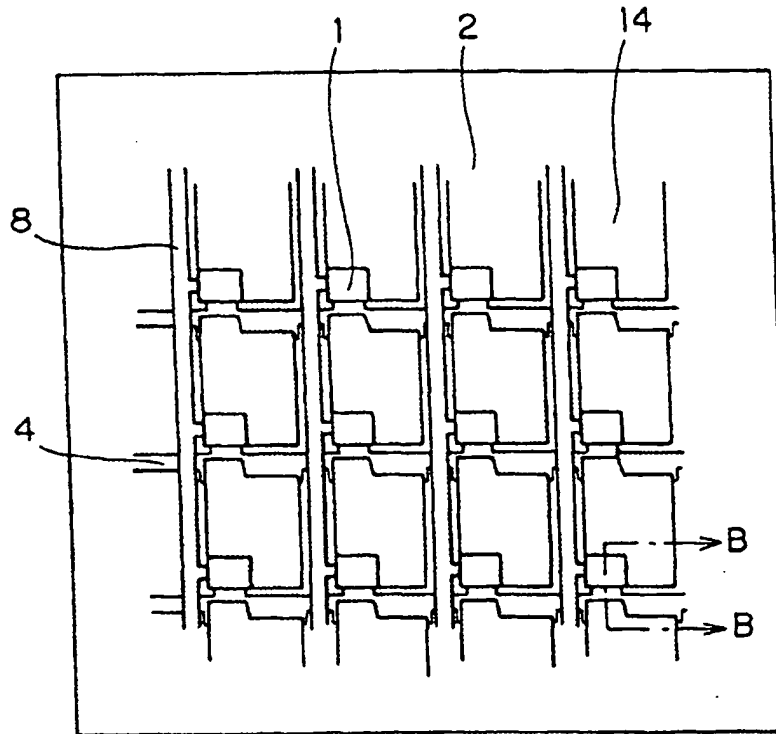


FIG.6

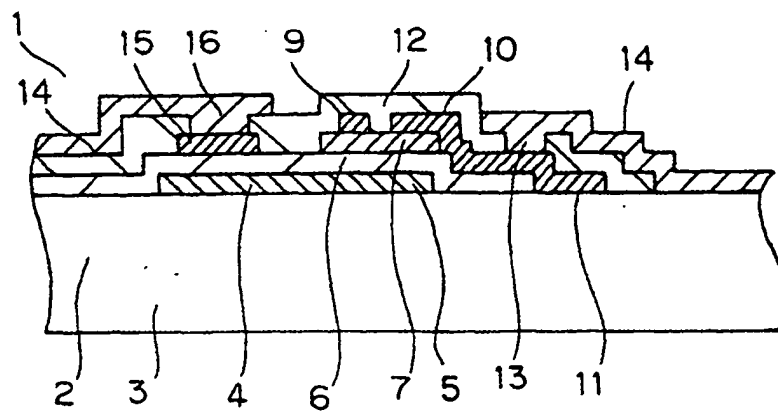


FIG.7

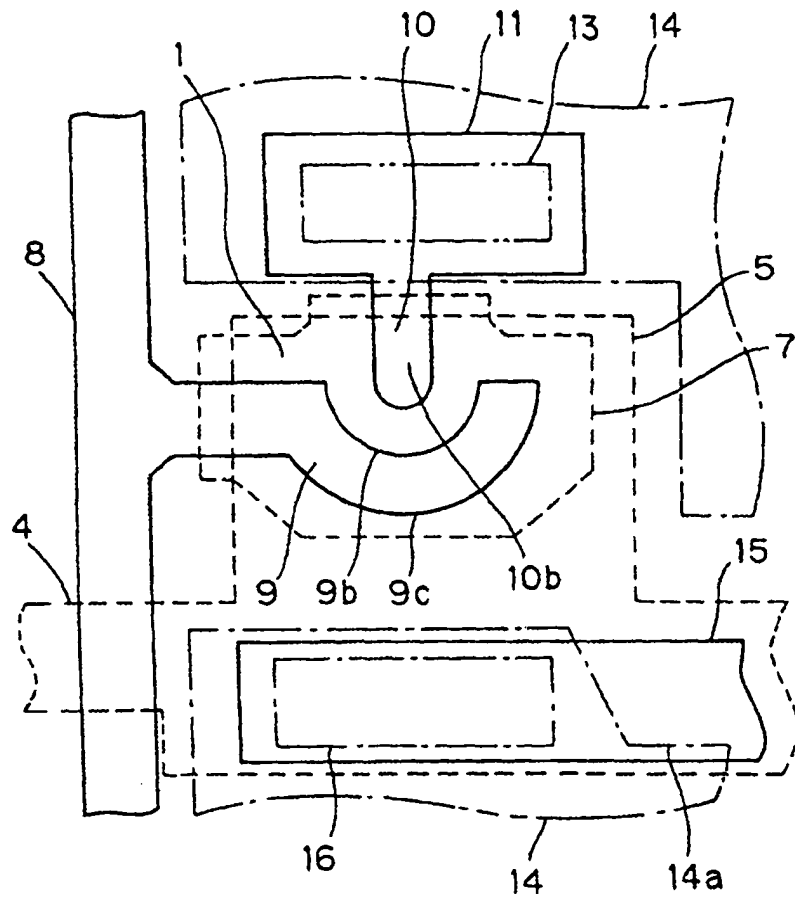


FIG.8

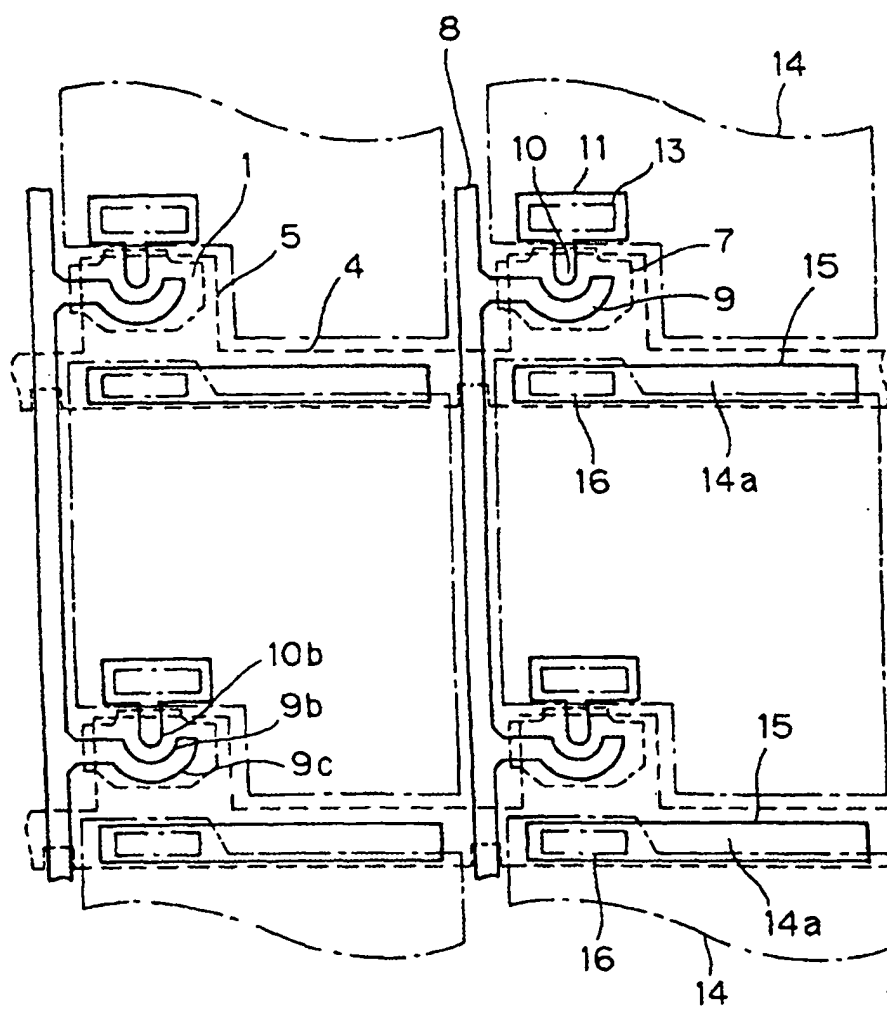


FIG. 9

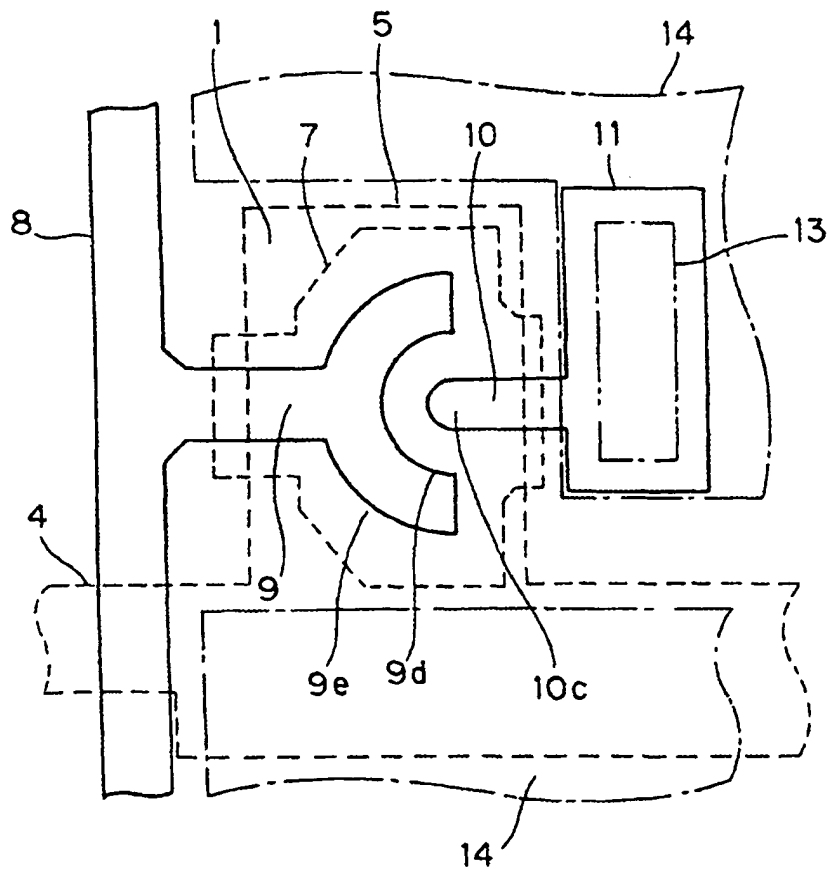


FIG. 10

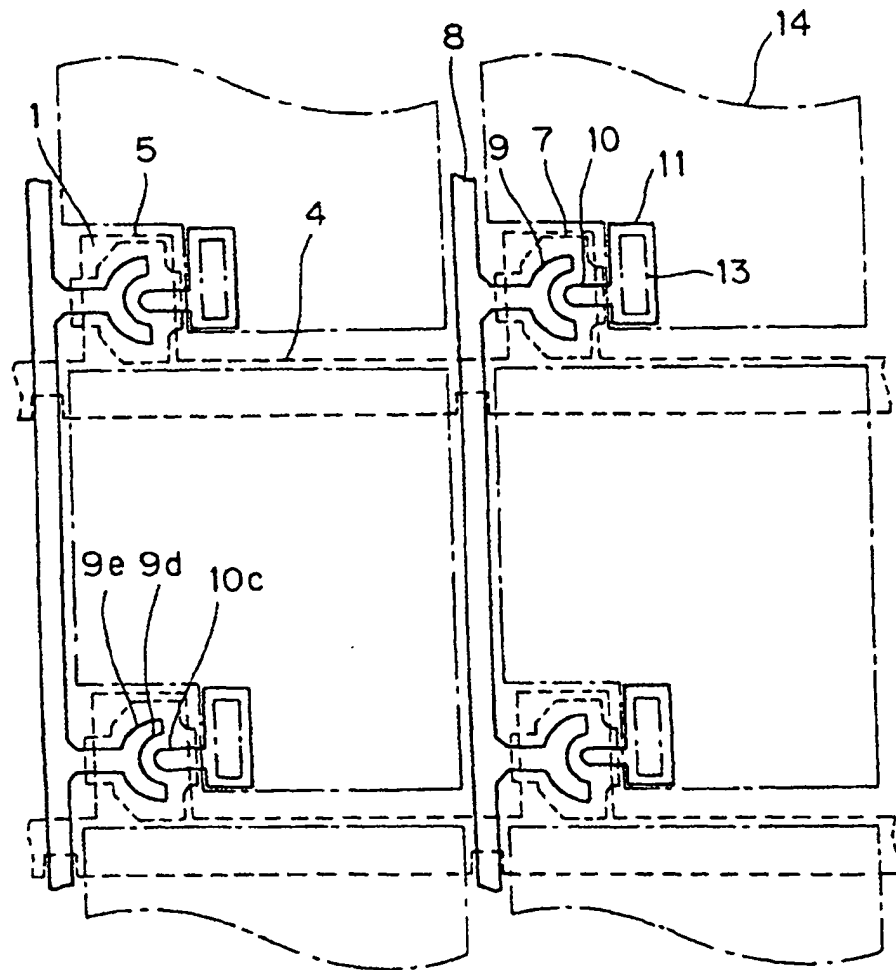


FIG.11

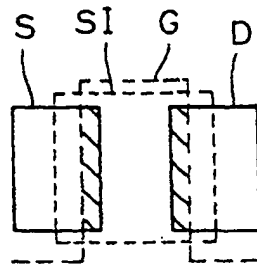


FIG.12

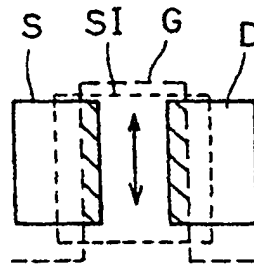
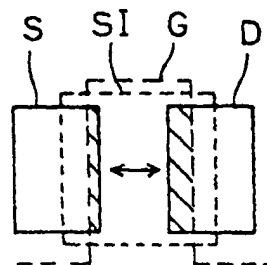


FIG.13



## INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP01/08867

<b>A. CLASSIFICATION OF SUBJECT MATTER</b> Int.Cl. <sup>7</sup> H01L29/786, H01L21/336, G02F1/1368		
According to International Patent Classification (IPC) or to both national classification and IPC		
<b>B. FIELDS SEARCHED</b> Minimum documentation searched (classification system followed by classification symbols) Int.Cl. <sup>7</sup> H01L29/786, H01L21/336, G02F1/1368		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Jitsuyo Shinan Koho 1922-1996 Toroku Jitsuyo Shinan Koho 1994-2001 Kokai Jitsuyo Shinan Koho 1971-2001 Jitsuyo Shinan Toroku Koho 1996-2001		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)		
<b>C. DOCUMENTS CONSIDERED TO BE RELEVANT</b>		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 2-285326 A (Toshiba Corporation), 22 November, 1990 (22.11.90), Full text	1-7 8
Y	Full text (Family: none)	
X	JP 2000-196098 A (Furontetsuku K.K.), 14 July, 2000 (14.07.00), Fig. 13	1,5 2-4,6-8
Y	Fig. 13 (Family: none)	
X	JP 60-189969 A (Matsushita Electric Industrial Co., Ltd.), 27 September, 1985 (27.09.85), Claim 2; Fig. 4	1,5,7 2-4,6,8
Y	Claim 2; Fig. 4 (Family: none)	
Y	JP 64-82674 A (Casio Computer Co., Ltd.), 28 March, 1989 (28.03.89), Claim 3; Fig. 1 & US 5003356 A	2-4,6
<input checked="" type="checkbox"/> Further documents are listed in the continuation of Box C. <input type="checkbox"/> See patent family annex.		
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier document but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search 19 December, 2001 (19.12.01)		Date of mailing of the international search report 15 January, 2002 (15.01.02)
Name and mailing address of the ISA/ Japanese Patent Office		Authorized officer
Facsimile No.		Telephone No.

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## INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP01/08867

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 6091464 A (LG Electronics, Inc.), 18 July, 2000 (18.07.00), Full text & JP 10-123572 A      & KR 247493 B & GB 2318445 A      & FR 2754917 A & DE 19746055 A	8
Y	JP 9-15642 A (NEC Corporation), 17 January, 1997 (17.01.97), Fig. 1 (Family: none)	8

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